YIYUN WANG

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Summary

Graduate international student in Electrical Engineering, specialized in analog/digital/mixed signal IC design, wafer processing integration and advanced packaging with cleanroom experiences, and embedded system design. Seeking internship opportunities related to hardware design, circuit design, and semiconductor fabrication.

Education

Purdue University West Lafayette, IN

- Master of Science in Electrical Engineering (MSEE) May 2026
  Concentration: Microelectronics, Semiconductors, and VLSI
- Bachelor of Science in Electrical Engineering (BSEE) May 2024
  Minor: Mathematics

Relevant Coursework:
Mixed signal circuit design, Embedded system, Solid state devices, Semiconductor through simulation, ASIC design Lab, Analog circuit design, IC/MEMS fabrication, Digital circuit design, Microprocessor system and design, Advanced packaging

Professional Experience

Internship in STARS Program – Minimum Feature Size Team May 2024 – July 2024
Research team lead in Purdue University Birck Nanotechnology Center West Lafayette, IN

- Fabricated wafers using lithography, PVD, and lift-off process with MGB-3 Mask Aligner and CHE-Beam PVD Evaporation Tool
- Assessed material characterization tools including microscopes and profilometer to accurately measure the minimum linewidth
- Applied problem-solving techniques and optimized a repeatable process, achieving stable 2μm chromium line patterning output
- Managed project schedules, supervised machine usage, and provided valuable feedback to improve lithography process parameters

Teaching Assistant for Electrical and Electronics Lab August 2022 – December 2022
Purdue University

- Provided weekly training and instruction to students on laboratory equipment operation, semiconductor fabrication processes, MOS (Metal-Oxide-Semiconductor) labs, and circuit analysis techniques
- Held regular office hours to provide academic support and meticulously graded lab reports, delivering constructive feedback to strengthen student understanding and performance

Teaching Assistant for Digital System Design May 2022 – August 2022
Purdue University

- Partnered with fellow teaching assistants to develop, organize, and refine course materials, monitoring alignment with learning objectives and curriculum standards
- Conducted weekly meetings with the professor to review and upgrade teaching materials.

Project Experience

MoldGuard development Project January 2025 – Present
Researcher under Prof. Babak Ziaie Purdue University

- Configured CO2 and BME688 sensors using Arduino IDE to support early-stage detection of mold growth (within 1-3 days)
- Designed and conducted mold growth experiments and integrated the data with AI Studio to develop predicting algorithms, enabling accurate forecasting and provide warning to the users

SONOS Device Compact Model Implementation Project September 2024 – December 2024
Researcher under Prof. Sumeet Gupta, Prof. David Jane and Skywater Technology Purdue University

- Explored SONOS compact model designs from Skywater technology undeveloped open source pdk and literature, gaining insights into advanced semiconductor device modeling
- Established and simulated spice model and Verilog-a physical model adhering to industrial standard
- Researched test patterns for post-fabrication experimentation, allowing future students to conduct research and analysis

Semiconductor@BirckHeterogeneous Integrated & Advanced Packaging (HI&AP) August 2023 – May 2024
Researcher under Prof. Zhihong Chen, Prof. Saeed Mohammadi VIP team Purdue University Birck Nanotechnology Center

- Investigated Aluminum Nitride (AlN) substrates in cleanroom environment to evaluate the functionality of advanced packaging
- Acquired hands-on experience by operating metrology characterization tools, including KLA alpha-step stylus profilometer and Bruker optical profilometer, for precise measurement to detect the defect on the surface and edge between substrate and die
- Brainstormed with the team by transitioning from copper to titanium, to enhance die-to-package bonding capability

8*8-bit Digital Multiplier Using Dadda Multiplier Architecture January 2024 – May 2024
Researcher Purdue University

- Conducted a comparative analysis of multiplier architectures (Dadda, Wallace-Tree, Carry-save) to select the most space-efficient design
- Assembled and implemented an 8*8-bit digital multiplier using the Dadda multiplier architecture, achieving high operational frequency (1GHz), low power dissipation (4.94mW), and minimal propagation delay (900ps)
- Verified the design using industry-standard EDA (Cadence Virtuoso) tools, finalized the paper and delivered a presentation

Fully Differential Amplifier and Common-Mode Feedback Design September 2023 – December 2023
Researcher Purdue University

- Built fully differential amplifier using wide-swing current source structure and current mirror amplified stage.
- Researched and developed deep triode common-mode feedback and dual-pair common-mode feedback system, achieving amplification effect of over 30dB, with 10mW power consumption, low noise and about 100MHz bandwidth.
- Simulated and optimized the circuit using EDA (Cadence Virtuoso) tools, finalized the paper and delivered a presentation

SOCET (System On Chip Extension Technology) Design Flow August 2022 – December 2022
Researcher under Prof. Mark Johnson SOCET team Purdue University

- Reviewed VLSI design flow focusing on synthesis, floor planning, and place-and-route, gaining understanding of IC development processes
- Engaged with the team to identify and resolve synthesis errors, leveraging Cadence tools to improve overall design quality
- Contributed to the presenting research findings at the Design Expo, collaborating with team members to prepare and deliver a public presentation that effectively communicated project outcomes and innovations

AHB_Lite_Slave USB Design Project August 2022 – December 2022
Research team lead Purdue University

- Supervise the project progress, coordinating sub-projects such as receiver, FIFO, and AHB_Lite_Slave design to ensure project is on time and alignment with overall project goals
- Developed AHB_Lite_Slave interface and testbench to assure accurate data transmission across addresses, achieving an 80% coverage rate
- Coordinated Integrated sub-project deliverables to uphold compliance with USB data transmission and storage requirements

Skills

- **Programming:** C, Python, MATLAB, System Verilog, Verilog-A, RTL. RISC-V, STM32, ESP32, Arduino, Micropython
- **Industrial-standard Tools:** Cadence Virtuoso, Klayout, HSPICE, LTSPICE, Silvaco TCAD
- **Semiconductor Fabrication:** Experience in Lithography, PVD, Lift-off, Microscopies, Profilometers, Cleanroom Environments
- **Languages:** English, Chinese (Mandarin), Germain

Leadership Experience

Toastmaster at Purdue 2022 – Present
Member/Ex-Sergeant at Arms Purdue University

- Delivered public speeches and impromptu speeches weekly and earned Toastmaster level 1 certificate
- Exercised leadership as Sergeant at Arms by organizing and managing technical setups for meetings and events, facilitating live streaming and accessibility for online participants
- Supported the club in achieving President's Distinguished Status by driving success in key areas, including membership growth, educational achievements, and effective operations.